**Remarks/Arguments:**

Claims 1, 5 and 13 have been amended. No new matter is introduced herein. Claims 1-5 and 7-14 are pending.

Claims 1-5, 7-9, 13 and 14 have been objected to for informalities therein. Claims 1, 5 and 13 have been amended as suggested by the Examiner. Accordingly, Applicants respectfully request that the objection to claims 1-5, 7-9, 13 and 14 be withdrawn.

Claims 1-5 and 7-12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Borg et al. (U.S. 6,476,864, referred to herein as Borg) in view of Henderson (U.S. 7,280,140) and further in view of Morse et al. (U.S. 4,786,831, referred to herein as Morse). Reconsideration is respectfully requested for the reasons set forth below.

Claim 1 includes features neither disclosed nor suggested by the cited art, namely:

> . . . the video circuit comprises a plurality of video amplifiers, each video amplifier is associated with a respective pixel in the row of pixels, each video amplifier includes a single capacitor having a terminal switched between a respective column input and an output of the video amplifier, and the video amplifiers sample in series, one at a time, the video voltage from each pixel in the row of pixels . . .(Emphasis added)

That is, a terminal of a single capacitor is switched between a respective column input and an output of the video amplifier. Claims 5 and 10 include similar recitations.

Borg discloses amplifiers 80 and 110. Amplifier 80 or amplifier 110 of Borg corresponds to the video amplifier recited in claim 1. Borg discloses that, during the first phase switches 76, 92 and 84 are closed. (See Borg at column 8, line 59 to column 9, line 6.) With switches 76, 92 and 84 closed, it is clear from FIG. 4 of Borg that capacitor 82 is connected between constant voltage reference Vref and the input of the amplifier 80 and capacitor 78 is connected between the column input and the input of the amplifier 80. Moreover, during the second phase, switches 92 and 84 are opened and switch 94 is closed. It is also clear from FIG. 4 of Borg that during the second phase capacitor 82 is connected between the input and output of amplifier 80.

As acknowledged by the Examiner on page 4 of the Office Action, Borg does not teach that each video amplifier includes a single capacitor having a terminal switched between a respective column input and an output of the video amplifier, as required by claim 1. Instead, Borg teaches the use of two capacitors (capacitors 78 and 82) for each amplifier. Thus, Borg does not include all of the features of claim 1.

Henderson discloses that an image sensor has an array of active pixels. Each column shares a reset voltage line VRT and a read line Vx. FIGs. 1 and 6 of Henderson show a Vsig capacitor 12 and a Vblk CDS capacitors 14. The voltage VRT-Vgsn is stored on the Vblk CDS capacitor 14 and the voltage VRT-Vgsn-Vrst-Vnrst is stored on the Vsig capacitor 12. (See Henderson at column 2, line 55-65.) The Vsig capacitor 12 and Vblk CDS capacitor 14 of Henderson each have a terminal connected to a column input.

As acknowledged by the Examiner on page 4 of the Office Action, Henderson does not teach that each video amplifier includes a single capacitor having a terminal switched between a respective column input and an output of the video amplifier, as required by claim 1. Henderson is silent regarding any switching of such a terminal to the output of an amplifier. Thus, Henderson does not make up for the deficiencies of Borg with respect to claim 1.

Morse discloses, in FIG. 3, infrared detector 10 connected to amplifier stage 12 by coupling capacitor 14. Detector 10 also includes integrating capacitor 18 connected across nodes 20, 22 of amplifier stage 12 (to provide integrating amplification of the output from detector 10) and capacitor reset switch 24 connected across nodes 20, 22 of integrating capacitor 18. (See Morse at column 2, line 53-column 3, line 5.) During a first time period, reset switch 16 and capacitor reset switch 24 are closed to initially bias detector 10 and initialize the integrating amplifier stage. During a second time period, detector reset switch 16 and capacitor reset switch 24 are opened, which places a voltage on amplifier output node 22. (See Morse at column 3, lines 6-25.) It is clear from FIG. 3 of Morse that during the second time period, node 20 is connected to output node 22 of amplifier stage 22 via integrating capacitor 18.

Morse, however, does not disclose or suggest that each video amplifier includes a single capacitor having a terminal switched between a respective column input and an output of the video amplifier, as required by claim 1. Morse is silent regarding this feature.

Contrary to the recitation in claim 1, Morse requires the use of two capacitors (coupling capacitor 14 and integrating capacitor 18). Thus, the terminal of coupling capacitor 14 (at node 20) cannot be switched between a respective column input and an output of the video amplifier, as required by claim 1. Accordingly, Morse does not make up for the deficiencies of Borg and Henderson with respect to claim 1. Accordingly, allowance of claim 1 is respectfully requested.

Although not identical to claim 1, claims 5 and 10 include features similar to claim 1 which are neither disclosed nor suggested by the cited art. Accordingly, allowance of claims 5 and 10 is respectfully requested for at least the same reasons as claim 1.

Claims 2-4, 7-9, 11 and 12 include all of the features of respective claims 1, 5 and 10 from which they depend. Accordingly, these claims are also patentable over the cited art for at least the same reasons as respective claims 1, 5 and 10.

Claims 13 and 14 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Henderson in view of Morse. Reconsideration is respectfully requested for the reasons set forth below.

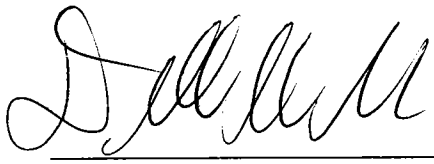
Claim 13, although not identical to claim 1, includes features similar to claim 1 which are neither disclosed nor suggested by the cited art. Namely, that the serial sampling of the video voltage by the video amplifier includes switching a terminal of a single capacitor between a respective column input and an output of the video amplifier. As discussed above, none of the cited art disclose or suggest this indicated feature. Accordingly, allowance of claim 13 is respectfully requested for at least the reasons set forth above with respect to claim 1.

Claim 14 includes all of the features of claim 13 from which it depends. Accordingly, claim 14 is also patentable over the cited art for at least the same reasons as claim 13.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

RatnerPrestia



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